ABSTRACT OF THE DISCLOSURE

[0079] A mapper circuit with backup capability. In one embodiment, the mapper circuit may store associations between physical register names (PRNs) and logical register names (LRNs) in a plurality of storage locations, each of the storage locations corresponding to a speculative state. One of the storage locations may store a LRN-to-PRN mappings for a current speculative state, while the other storage locations may store LRN-to-PRN mappings for previous speculative states. In a case where the processor is required to back up (e.g., such as in the case of a branch misprediction), one of the mappings associated with a previous speculative state may be reverted to an association with the current speculative state.